

IBM DOCKET: FIS920010192US1

## PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

|              |  |   |           |                   |
|--------------|--|---|-----------|-------------------|
| INVENTOR:    | Christopher P. Ausschnitt et al.   | ) | EXAMINER: |                   |
| SERIAL NO.:  | 09/977,793   | ) | ART UNIT: | 2877              |
| FILING DATE: | October 15, 2001   | ) | DATE:     | February 15, 2002 |
| FOR:         | Method For Determining<br>Semiconductor Overlay on<br>Groundrule Devices | ) |           |                   |

## INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

In accordance with 37 CFR 1.56, 1.97 and 1.98, the following items are made of record to assist the Patent & Trademark Office in its examination of this application and is, in the opinion of the attorney designated below for applicant(s), information relevant to the closest prior art of which that person is aware. The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or that no other art than that identified exists.

**PATENT NO.**

5,545,593  
5,877,861

**INVENTOR**

Watkins et al.  
Ausschnitt et al.

**ISSUE DATE**

August 13, 1996  
March 2, 1999

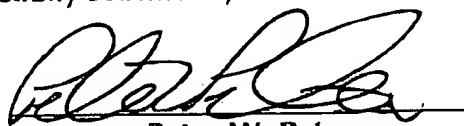
IBM Docket No. FIS920010192US1

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A copy of each of the foregoing items and Form PTO 1449 are enclosed  
herewith.

Respectfully submitted,

By:

Attorney: **Peter W. Peterson**Reg. No.: **31,867**

DeLIO & PETERSON, LLC  
121 Whitney Avenue  
New Haven, CT 06510  
(203) 787-0595

## CERTIFICATE OF MAILING UNDER 37 CFR 1.10

I hereby certify that, on the date shown below, this correspondence is being deposited with the United States Postal Service in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, as first class mail by:

Name: Barbara BrowneDate: February 15, 2002Signature: 

ibmf100342000ids1

IBM DOCKET: FIS920010192US1

PATENT

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|              |                          |   |           |                |
|--------------|--------------------------|---|-----------|----------------|
| INVENTOR:    | C. Ausschnitt et al.     | ) | EXAMINER: |                |
|              |                          | ) |           |                |
| SERIAL NO.:  | 09/977,793               | ) | ART UNIT: | 2877           |
|              |                          | ) |           |                |
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|              |                          | ) |           |                |
| FOR:         | Method for Determining   | ) |           |                |
|              | Semiconductor Overlay on | ) |           |                |
|              | Groundrule Devices       | ) |           |                |

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

In accordance with 37 CFR 1.56, 1.97 and 1.98, the following items are made of record to assist the Patent & Trademark Office in its examination of this application and is, in the opinion of the attorney designated below for applicant(s), information relevant to the closest prior art of which that person is aware. The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or that no other art than that identified exists.

| <b><u>PATENT NO.</u></b> | <b><u>INVENTOR</u></b> | <b><u>ISSUE DATE</u></b> |
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"Method for Measuring Semiconductor Lithographic Tool Focus and Exposure", IBM Technical Disclosure Bulletin, July 1987, pages 516-518.

A copy of each of the foregoing items and Form PTO 1449 are enclosed herewith.

Respectfully submitted,

By:



Attorney: **Peter W. Peterson**

Reg. No.: **31,867**

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Name: Barbara Browne  
ibmf100342000supp ids1

Date: March 15, 2002

Signature: 

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-2-

**PATENT NO.**

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**INVENTOR**

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February 12, 2002

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Japan  
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